Models and Peterson's Algorithm

This is Peterson's algorithm:

```
boolean[] enter = {false, false};   int yield = 0 || 1;
```

thread t_0

```
1 while (true) {
2  // entry protocol
3  enter[0] = true;
4  yield = 0;
5  await (!enter[1]
         || yield != 0);
6  critical section { ... }
7  // exit protocol
8  enter[0] = false;
9 }
```

thread t_1

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while (true) {                  10
 // entry protocol              11
 enter[1] = true;               12
 yield = 1;                     13
 await (!enter[0]               14
        || yield != 1);
 critical section { ... }       15
 // exit protocol               16
 enter[1] = false;              17
}                               18
```

The successors of $\langle yield = 0, \triangleright 6, enter[0] = T, \triangleright 14, enter[1] = T \rangle$ are:

1. The t_0 successor is $\langle yield = 0, \triangleright 3, enter[0] = F, \triangleright 14, enter[1] = T \rangle$.
2. The t_0 successor is $\langle yield = 0, \triangleright 8, enter[0] = T, \triangleright 14, enter[1] = T \rangle$.
3. The t_1 successor is $\langle yield = 0, \triangleright 6, enter[0] = T, \triangleright 15, enter[1] = T \rangle$.
4. There is no t_1 successor.

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- State $\langle \mathit{yield} = 0, \triangleright 6, \mathit{enter}[0] = T, \triangleright 14, \mathit{enter}[1] = T \rangle$ does not exist.
- There is a bug in Peterson's algorithm.
- The previous slide was wrong.
- State $\langle \mathit{yield} = 0, \triangleright 6, \mathit{enter}[0] = T, \triangleright 14, \mathit{enter}[1] = T \rangle$ is never entered.

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What does Peterson's algorithm achieve?

1. Mutual exclusion using only atomic reads and writes
2. Mutual exclusion and first-come-first-served fairness
3. Mutual exclusion using busy waiting
4. Mutul exclusion using test-and-set operations

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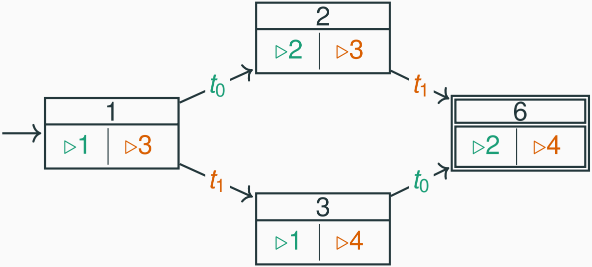
What properties does the following state/transition diagram show?



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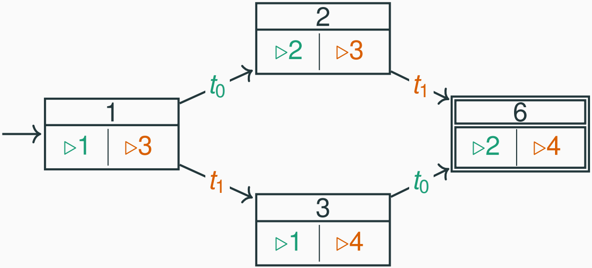

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